19-2489; Rev 1; 9/02

825MHz to 915MHz, SiGe High-Linearity Active Mixer

MAX9982

General Description

The MAX9982 fully integrated SiGe mixer is optimized to meet the demanding requirements of GSM850, GSM900, and CDMA850 base-station receivers. Each high-linearity device includes a local oscillator (LO) switch, LO driver, and active mixer. On-chip baluns are also integrated to allow for single-ended RF and LO inputs. Since the active mixer provides 2dB of conversion gain, the device effectively replaces the IF amplifier stage, which typically follows most passive mixer implementations.

The MAX9982 provides exceptional linearity with an input IP3 of greater than +26dBm. The integrated LO driver allows for a wide range of LO drive levels from -5dBm to +5dBm. In addition, the built-in switch enables rapid LO selection of less than 250ns, as needed for GSM frequency-hopping applications.

The MAX9982 is available in a 20-pin QFN package (5mm × 5mm) with an exposed paddle and is specified over the -40°C to +85°C extended temperature range.

Applications

GSM850/GSM900 2G and 2.5G EDGE Base Station Receivers

Cellular cdmaOne™ and cdma2000™ Base Station Receivers

TDMA and Integrated Digital Enhanced Network (iDEN)™ Base Station Receivers

Digital and Spread-Spectrum Communication Systems

Microwave Links

Typical Application Circuit appears at end of data sheet.

cdmaOne is a trademark of CDMA Development Group.

cdma2000 is a trademark of Telecommunications Industry Association.

iDEN is a trademark of Motorola, Inc.

Features

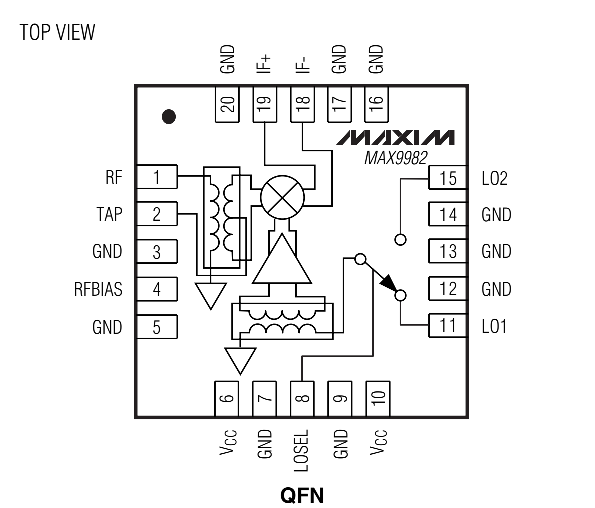
- ♦ **+26.8dBm Input IP3**
- ♦ **+13dBm Input 1dB Compression Point**
- ♦ **825MHz to 915MHz RF Frequency Range**
- ♦ **70MHz to 170MHz IF Frequency Range**
- ♦ **725MHz to 1085MHz LO Frequency Range**
- ♦ **2dB Conversion Gain**
- ♦ **12dB Noise Figure**
- ♦ **-5dBm to +5dBm LO Drive**
- ♦ **5V Single-Supply Operation**
- ♦ **Built-In LO Switch**
- ♦ **ESD Protection**
- ♦ **Internal RF and LO Baluns for Single-Ended Inputs**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9982ETP	-40°C to +85°C	20 QFN-EP* (5mm × 5mm)

**EP = exposed paddle.*

Pin Configuration/ Functional Diagram



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

825MHz to 915MHz, SiGe High-Linearity Active Mixer

ABSOLUTE MAXIMUM RATINGS

V_{CC} ....-0.3V to +5.5V
IF+, IF-, RFBIAS, LOSEL............................-0.3V to (V_{CC} + 0.3V)
TAP ....+5.0V
RFBIAS Current...5mA
RF, LO1, LO2 Input Power ....+20dBm
Continuous Power Dissipation (T_A = +70°C)
20-Pin QFN (derate 20.8mW/°C above T_A = +70°C) 1.66W
Operating Temperature Range ....-40°C to +85°C
Junction Temperature...+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = 4.75V to 5.25V, no RF signals applied, all RF inputs and outputs terminated with 50Ω, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5.00	5.25	V
Supply Current	I_{CC}		138	168	193	mA
Input High Voltage	V_{IH}		3.5		V_{CC} + 0.3V	V
Input Low Voltage	V_{IL}				0.4	V
LOSEL Input Current	I_{LOSEL}		-5		+5	µA

AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, V_{CC} = 4.75V to 5.25V, P_{LO} = -5dBm to +5dBm, f_{RF} = 825MHz to 915MHz, f_{LO} = 725MHz to 1085MHz, T_A = -40°C to +85°C, unless otherwise noted. Typical values at V_{CC} = +5.0V, P_{RF} = -5dBm, P_{LO} = 0dBm, f_{RF} = 870MHz, f_{LO} = 770MHz, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RF Frequency	f_{RF}			825		915	MHz
LO Frequency	f_{LO}			725		1085	MHz
IF Frequency	f_{IF}	Must meet RF and LO frequency range; IF matching components affect IF frequency range		70		170	MHz
LO Drive Level	P_{LO}			-5		+5	dBm
Conversion Gain (Note 3)	G_C	V_{CC} = +5.0V, f_{IF} = 100MHz, low-side injection, P_{RF} = 0dBm, P_{LO} = -5dBm	Cellular band, f_{RF} = 825MHz to 850MHz		2.6		dB
			GSM band, f_{RF} = 880MHz to 915MHz		2.1		dB
Gain Variation Over Temperature		T_A = -40°C to +85°C			-0.0135		dB/°C
Gain Variation from Nominal		f_{RF} = 825MHz to 915MHz, 3σ			±0.6		dB

AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit*, V_{CC} = 4.75V to 5.25V, P_{LO} = -5dBm to +5dBm, f_{RF} = 825MHz to 915MHz, f_{LO} = 725MHz to 1085MHz, T_A = -40°C to +85°C, unless otherwise noted. Typical values at V_{CC} = +5.0V, P_{RF} = -5dBm, P_{LO} = 0dBm, f_{RF} = 870MHz, f_{LO} = 770MHz, T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Conversion Loss from LO to IF		Inject P_{IN} = -20dBm at f_{LO} + 100MHz into LO port; measure 100MHz at IF port as P_{OUT}; no RF signal at RF port			47		dB
Noise Figure	NF	Cellular band, f_{RF} = 825MHz to 850MHz			11.3		dB
		GSM band, f_{RF} = 880MHz to 915MHz			11.8		
Input 1dB Compression Point	P_{1dB}	Low-side injection			12.9		dBm
		High-side injection			14.5		
Input Third-Order Intercept Point	IIP3	V_{CC} = +5.0V, P_{RF} = 0dBm, P_{LO} = -5dBm, T_A = +25°C (Notes 3, 4)			26.8		dBm
Input Third-Order Intercept Point Variation Over Temperature	ΔIIP3	T_A = -40°C to +85°C			±0.5		dB
2 RF - 2 LO Spur Rejection	2 × 2	f_{RF} = 915, f_{LO} = 815MHz, f_{SPUR} = 865MHz, P_{RF} = -5dBm	P_{LO} = +5dBm		65		dBc
			P_{LO} = 0dBm		57		
3 RF - 3 LO Spur Rejection	3 × 3	f_{RF} = 915, f_{LO} = 815MHz, f_{SPUR} = 848.3MHz, P_{RF} = -5dBm	P_{LO} = +5dBm		89		dBc
			P_{LO} = 0dBm		89		
Maximum LO Leakage at RF Port		P_{LO} = -5dBm to +5dBm, f_{LO} = 725MHz to 1085MHz			-40		dBm
Maximum LO Leakage at IF Port		P_{LO} = -5dBm to +5dBm, f_{LO} = 725MHz to 1085MHz			-28		dBm
Minimum RF to IF Isolation		P_{LO} = -5dBm to +5dBm, f_{RF} = 825MHz to 915MHz			11		dB
LO1 to LO2 Isolation		f_{RF} = 825MHz to 915MHz, P_{LO1} = P_{LO2} = +5dBm, f_{IF} = 100MHz (Note 5)			51		dB
LO Switching Time		50% of LOSEL to IF settled within 2°			250		ns
RF Return Loss					19		dB
LO Return Loss		LO port active			20		dB
		LO port inactive			12		
IF Return Loss		RF and LO terminated (Note 6)			15		dB

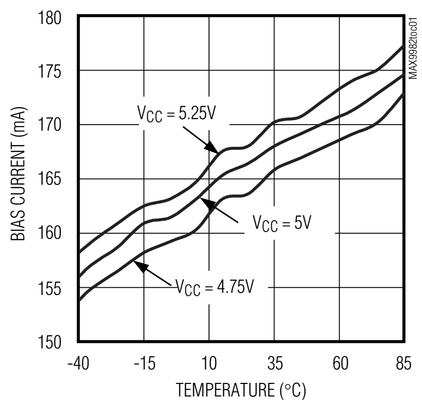
Note 1: Guaranteed by design and characterization.
Note 2: All limits reflect losses of external components. Output measurements taken at IF OUT of *Typical Application Circuit*.
Note 3: Production tested.
Note 4: Two tones at 1MHz spacing, 0dBm each at RF port.
Note 5: Measured at IF port at IF frequency. LO1 and LO2 are offset by 1MHz.
Note 6: IF return loss can be optimized by external matching components.

825MHz to 915MHz, SiGe High-Linearity Active Mixer

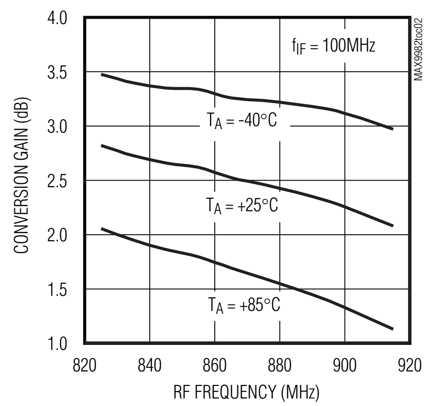
Typical Operating Characteristics

(*Typical Application Circuit*, V_{CC} = 5V, f_{IF} = 100MHz, P_{RF} = -5dBm, P_{LO} = 0dBm, T_A = +25°C, unless otherwise noted.)

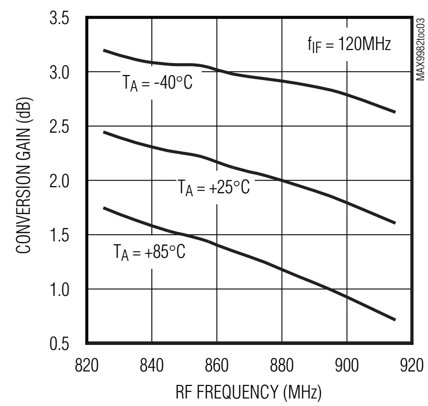
BIAS CURRENT vs. TEMPERATURE



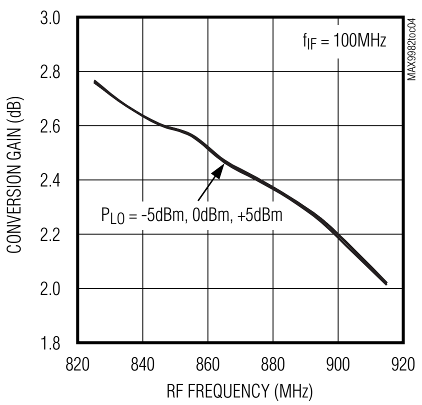
CONVERSION GAIN vs. RF FREQUENCY LOW-SIDE INJECTION



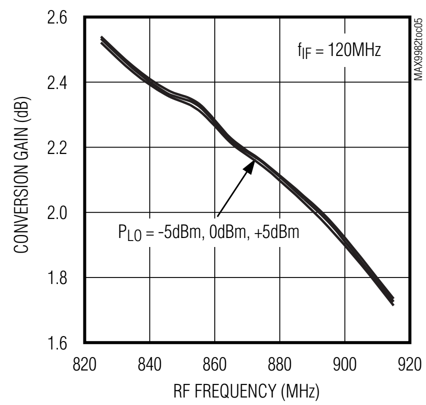
CONVERSION GAIN vs. RF FREQUENCY HIGH-SIDE INJECTION



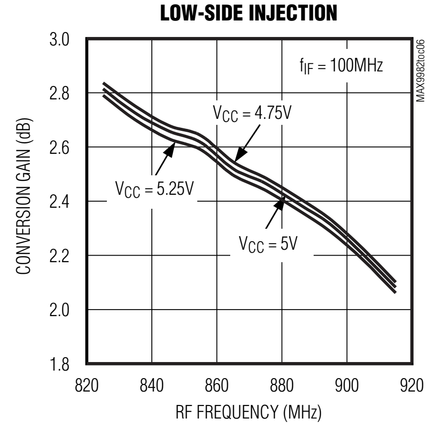
CONVERSION GAIN vs. RF FREQUENCY LOW-SIDE INJECTION



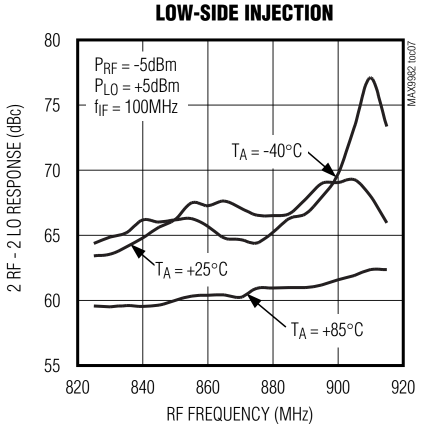
CONVERSION GAIN vs. RF FREQUENCY HIGH-SIDE INJECTION



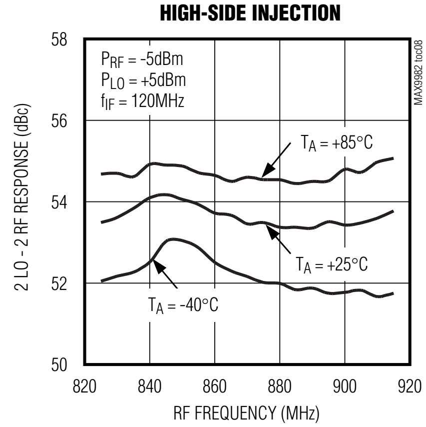
CONVERSION GAIN vs. RF FREQUENCY LOW-SIDE INJECTION



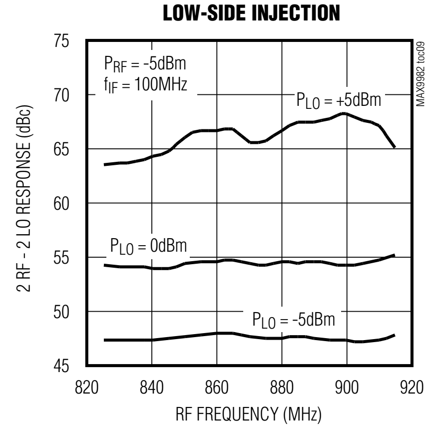
2 RF - 2 LO vs. RF FREQUENCY LOW-SIDE INJECTION



2 LO - 2 RF RESPONSE vs. RF FREQUENCY HIGH-SIDE INJECTION



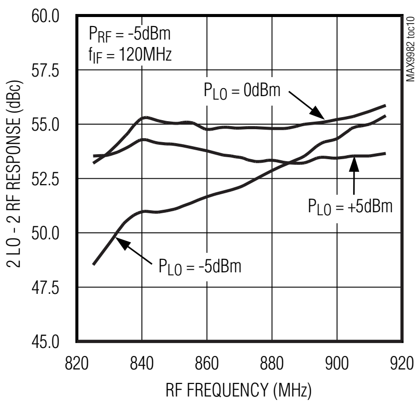
2 RF - 2 LO RESPONSE vs. RF FREQUENCY LOW-SIDE INJECTION



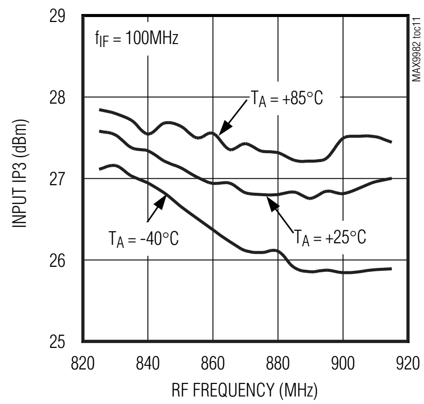
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CC} = 5V, f_{IF} = 100MHz, P_{RF} = -5dBm, P_{LO} = 0dBm, T_A = +25°C, unless otherwise noted.)

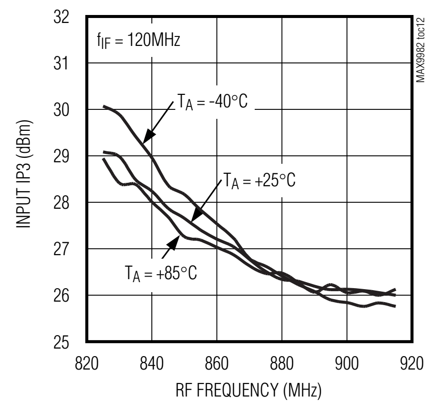
2 LO - 2 RF RESPONSE vs. RF FREQUENCY HIGH-SIDE INJECTION



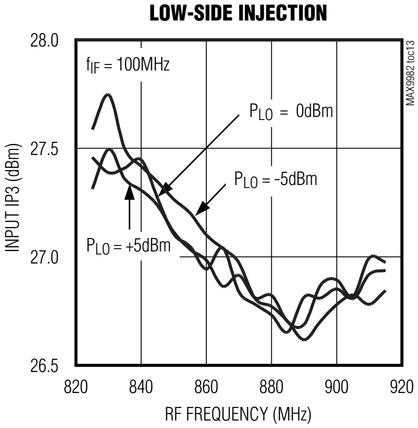
INPUT IP3 vs. RF FREQUENCY LOW-SIDE INJECTION



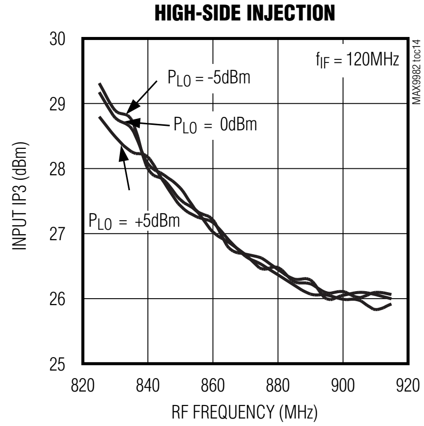
INPUT IP3 vs. RF FREQUENCY HIGH-SIDE INJECTION



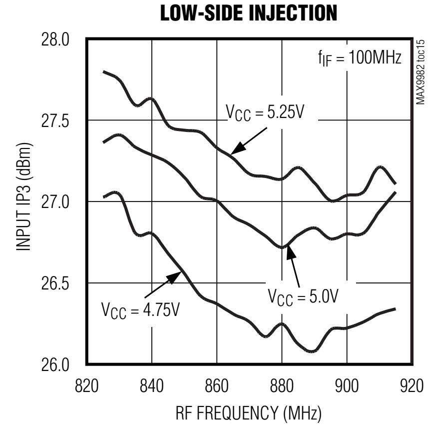
INPUT IP3 vs. RF FREQUENCY LOW-SIDE INJECTION



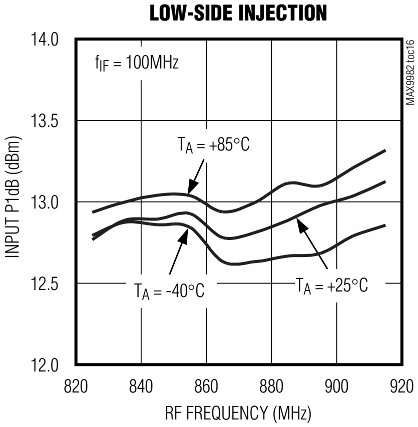
INPUT IP3 vs. RF FREQUENCY HIGH-SIDE INJECTION



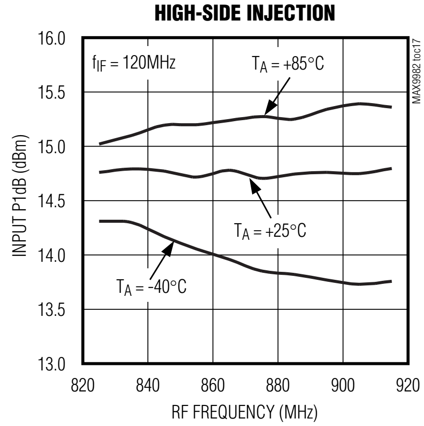
INPUT IP3 vs. RF FREQUENCY LOW-SIDE INJECTION



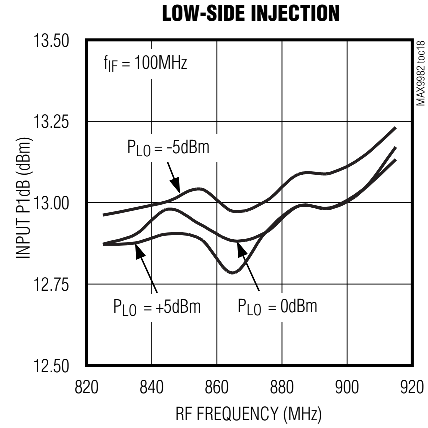
INPUT P1dB vs. RF FREQUENCY LOW-SIDE INJECTION



INPUT P1dB vs. RF FREQUENCY HIGH-SIDE INJECTION



INPUT P1dB vs. RF FREQUENCY LOW-SIDE INJECTION

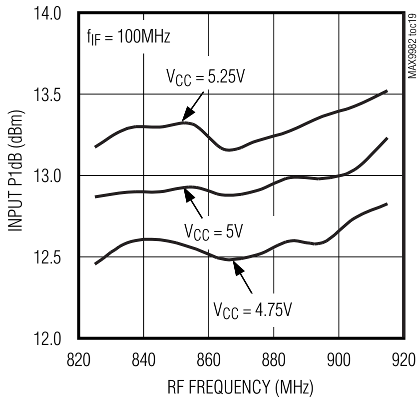


825MHz to 915MHz, SiGe High-Linearity Active Mixer

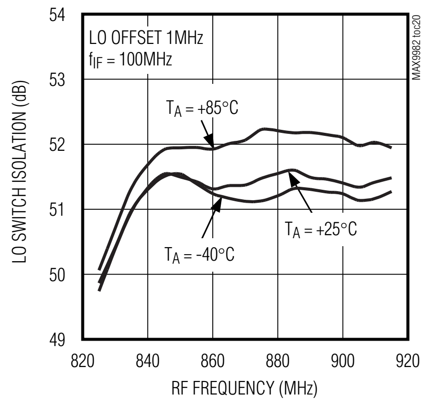
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CC} = 5V, f_{IF} = 100MHz, P_{RF} = -5dBm, P_{LO} = 0dBm, T_A = +25°C, unless otherwise noted.)

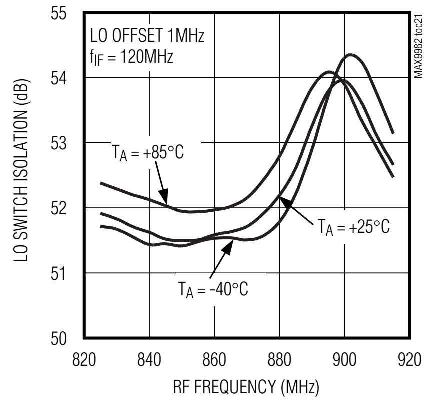
INPUT P1dB vs. RF FREQUENCY
LOW-SIDE INJECTION



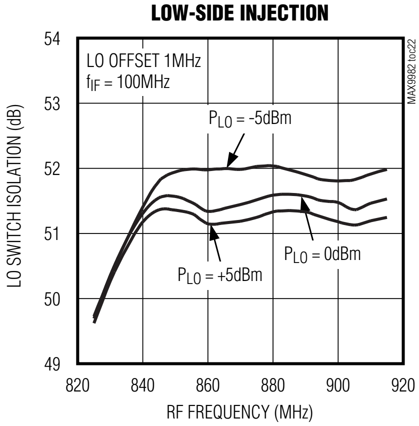
LO SWITCH ISOLATION vs. RF FREQUENCY
LOW-SIDE INJECTION



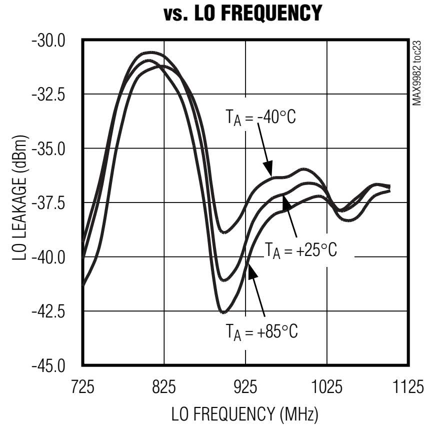
LO SWITCH ISOLATION vs. RF FREQUENCY
HIGH-SIDE INJECTION



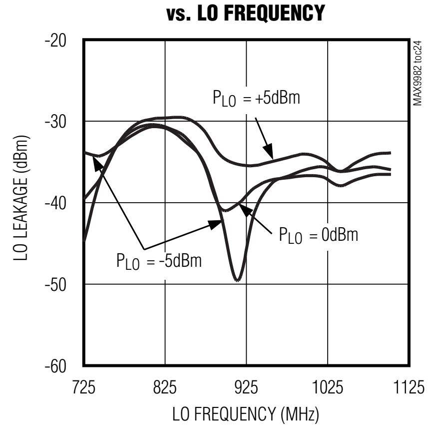
LO SWITCH ISOLATION vs. RF FREQUENCY
LOW-SIDE INJECTION



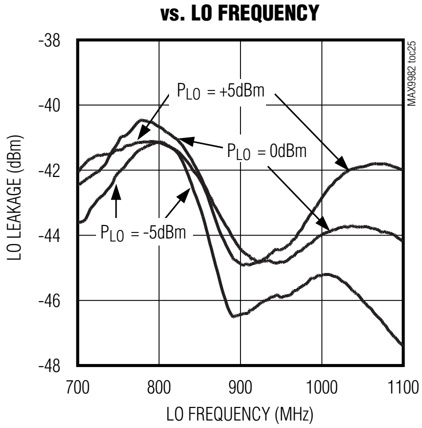
LO LEAKAGE AT IF PORT
vs. LO FREQUENCY



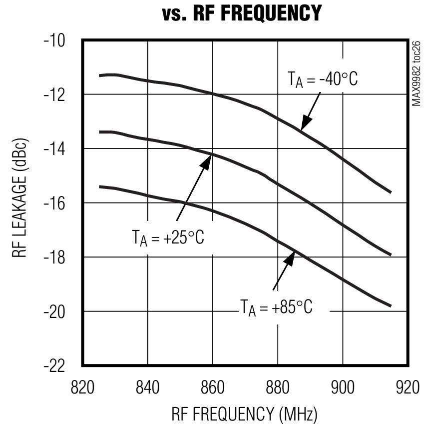
LO LEAKAGE AT IF PORT
vs. LO FREQUENCY



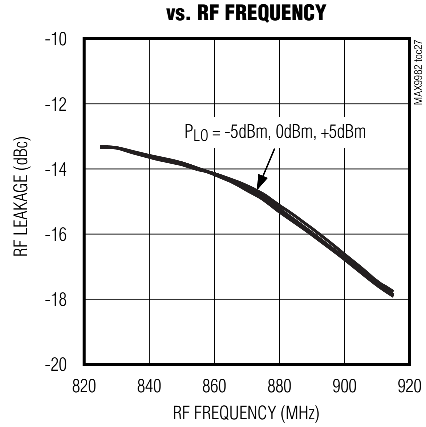
LO LEAKAGE AT RF PORT
vs. LO FREQUENCY



RF LEAKAGE AT IF PORT
vs. RF FREQUENCY



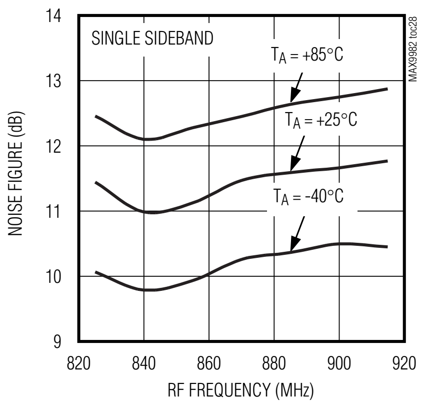
RF LEAKAGE AT IF PORT
vs. RF FREQUENCY



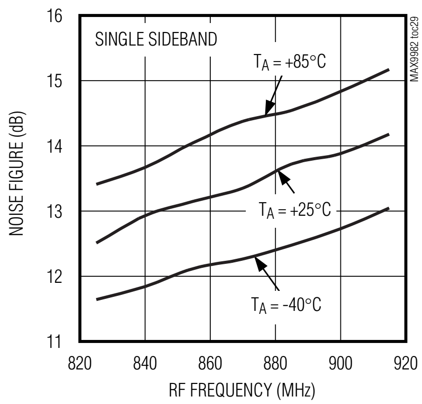
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CC} = 5V, f_{IF} = 100MHz, P_{RF} = -5dBm, P_{LO} = 0dBm, T_A = +25°C, unless otherwise noted.)

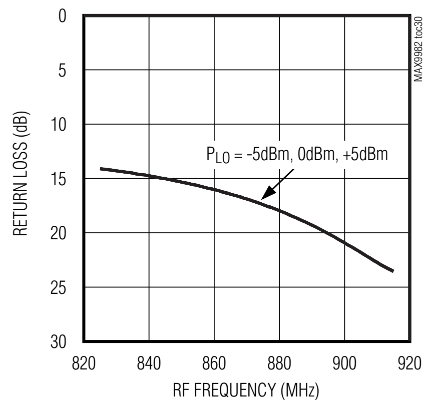
NOISE FIGURE vs. RF FREQUENCY LOW-SIDE INJECTION



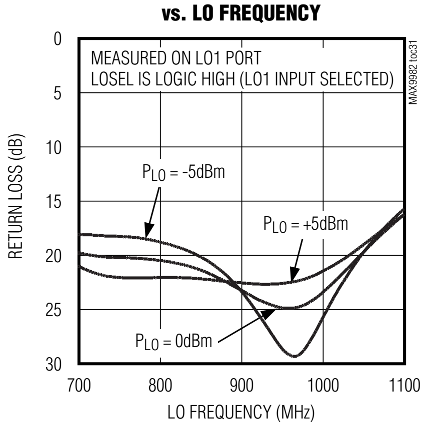
NOISE FIGURE vs. RF FREQUENCY HIGH-SIDE INJECTION



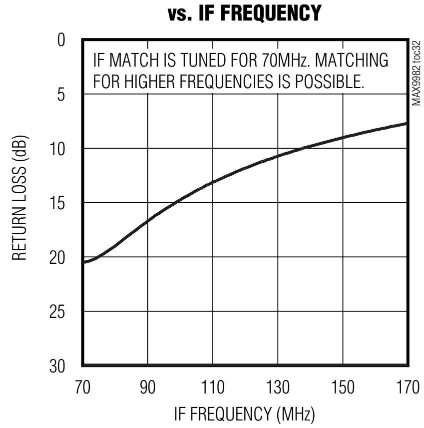
RF RETURN LOSS vs. RF FREQUENCY



LO RETURN LOSS vs. LO FREQUENCY



IF RETURN LOSS vs. IF FREQUENCY



825MHz to 915MHz, SiGe High-Linearity Active Mixer

Pin Description

PIN	NAME	FUNCTION
1	RF	RF Input. This input is internally matched to 50Ω and is DC shorted to ground.
2	TAP	RF Balun Center Tap. Connect bypass capacitors from this pin to ground.
3, 5, 7, 9, 12, 13, 14, 16, 17, 20, EP	GND	Ground
4	RFBIAS	Bias control for the mixer. Connect a 249Ω resistor from this pin to ground to set the bias current for the mixer.
6, 10	V_{CC}	Power-Supply Connections. Connect a 0.1µF bypass capacitor from each V_{CC} pin to ground.
8	LOSEL	Local Oscillator Select. Set this pin to logic HIGH to select LO1; set to logic LOW to select LO2.
11	LO1	Local Oscillator Input 1. This input is internally matched to 50Ω and is DC shorted to ground when selected. Requires a DC-blocking capacitor.
15	LO2	Local Oscillator Input 2. This input is internally matched to 50Ω and is DC shorted to ground when selected.
18, 19	IF-, IF+	Differential IF Output. Connect 560nH pullup inductors and 137Ω pullup resistors from each of these pins to V_{CC} for a 70MHz to 120MHz IF range.

Table 1. Component List

COMPONENT	VALUE	SIZE	PART
C1, C2, C6, C7	33pF	0603	Murata GRM1885C1H330J
C3	0.033µF	0603	Murata GRM188R71E333K
C4, C5	0.1µF	0603	Murata GRM188FS1E104Z
C8, C11	220pF	0603	Murata GRM1885C1H221J
C9, C10	330pF	0603	Murata GRM1885C1H331J
L1, L2	560nH	1008	Coilcraft 1008CS-561XJBB
R1	249Ω ±1%	0603	Panasonic ERJ-3EKF2490V
R3, R4	137Ω ±1%	0603	Panasonic ERJ-3EKF1370V
T1	4:1 (200:50)	—	Mini-Circuits TC4-1W-7A
U1	—	20-pin 5mm x 5mm QFN	MAX9982ETP

Detailed Description

The MAX9982 downconverter mixer is designed for GSM and CDMA base station receivers with an RF frequency between 825MHz and 915MHz. It implements an active mixer that provides 2dB of overall conversion gain to the receive path, removing the need for an additional IF amplifier. The mixer has excellent input IP3 measuring +26.8dBm. The device also features integrated RF and LO baluns that allow the mixers to be driven with single-ended signals.

RF Inputs

The MAX9982 has one input (RF) that is internally matched to 50Ω requiring no external matching components. A 33pF DC-blocking capacitor is required at the input since the input is internally DC shorted to ground through a balun. The input frequency range is 825MHz to 915MHz.

LO Inputs

The mixer can be used for either high-side or low-side injection applications with an LO frequency range of

725MHz to 1085MHz. An internal LO switch allows for switching between two single-ended LO ports; this is useful for fast frequency changes/frequency hopping. LO switching time is typically less than 250ns. The switch is controlled by a digital input (LOSEL) that when high, selects LO1 and when low, selects LO2.

Internal LO buffers allow for a wide power range on the LO ports. The LO signal power can vary from -5dBm to +5dBm. LO1 and LO2 are internally matched to 50Ω, so only a 33pF DC-blocking capacitor is required at each LO port.

IF Outputs

This mixer has an IF frequency range of 70MHz to 170MHz. The differential IF output ports require external pullup inductors to V_{CC} to resonate out the differential on-chip capacitance of 1.8pF. See the *Typical Application Circuit* for recommended component values for an IF optimized for 70MHz to 100MHz. Higher IF frequencies can be optimized by reducing the values of L1 and L2.

Removing the ground plane from underneath L1 and L2 reduces parasitic capacitive loading and improves VSWR.

Bias Circuitry

Connect a bias resistor from RFBIAS to ground to set the mixer bias current. A nominal resistor value of 249Ω sets an input IP3 of +26.8dBm and supply current of 168mA.

Applications Information

Layout Considerations

A properly designed PC board is an essential part of any RF/microwave circuit. Keep RF signal lines as short as possible to reduce losses, radiation, and inductance. For best performance, route the ground pin traces directly to the exposed paddle underneath the package. Solder the exposed pad on the bottom of the device package evenly to the board ground plane to provide a heat transfer path along with RF grounding. If the PC board ground plane is not immediately available on the top metal layer, provide multiple vias between the exposed paddle connection and the PC board ground plane.

Power-Supply Bypassing

Proper voltage supply bypassing is essential for high-frequency circuit stability. Bypass each V_{CC} pin with a 0.1µF capacitor. Bypass TAP by placing a 33pF (C2) to ground within 100 mils of the TAP pin.

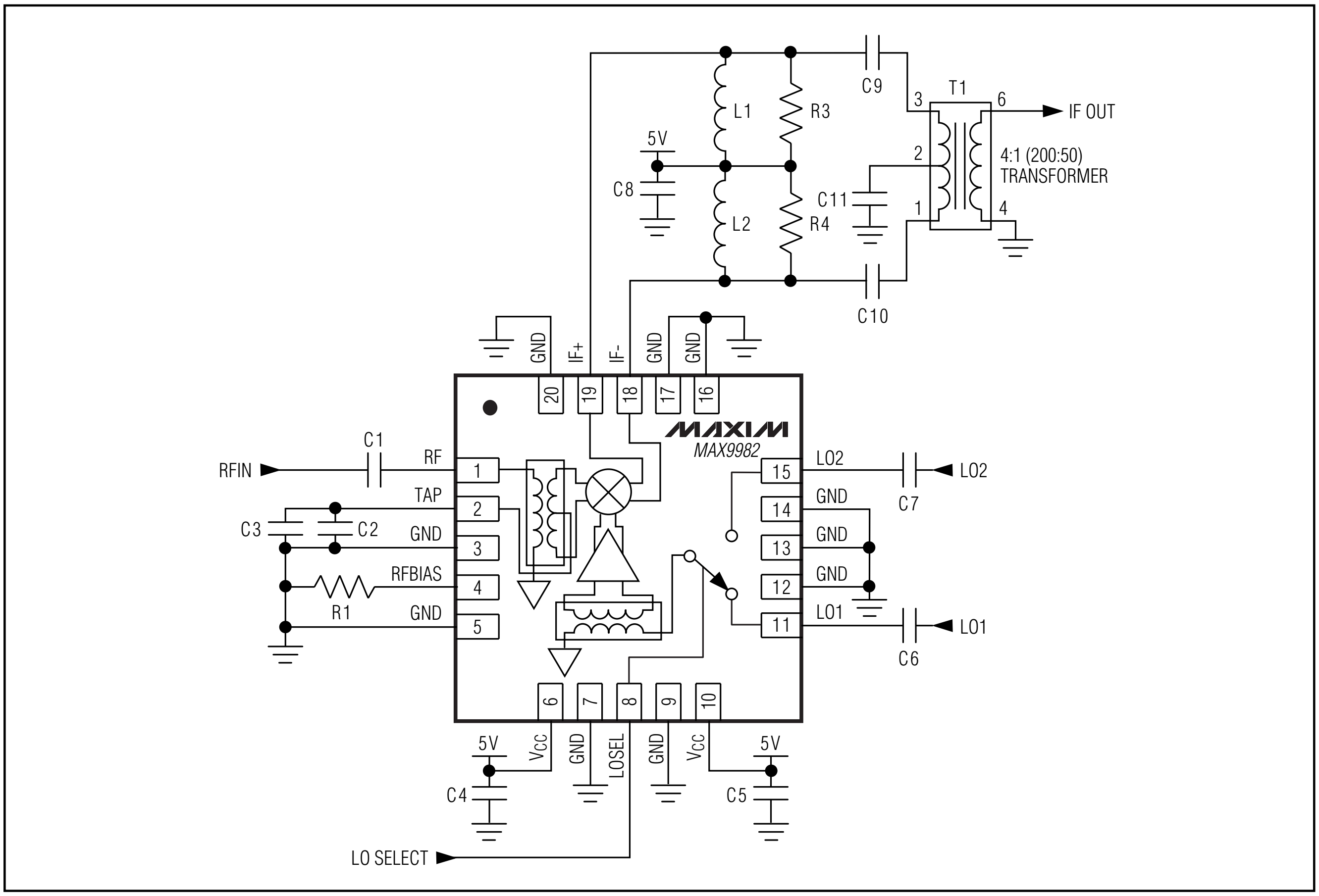
Chip Information

TRANSISTOR COUNT: 179

PROCESS: BiCMOS

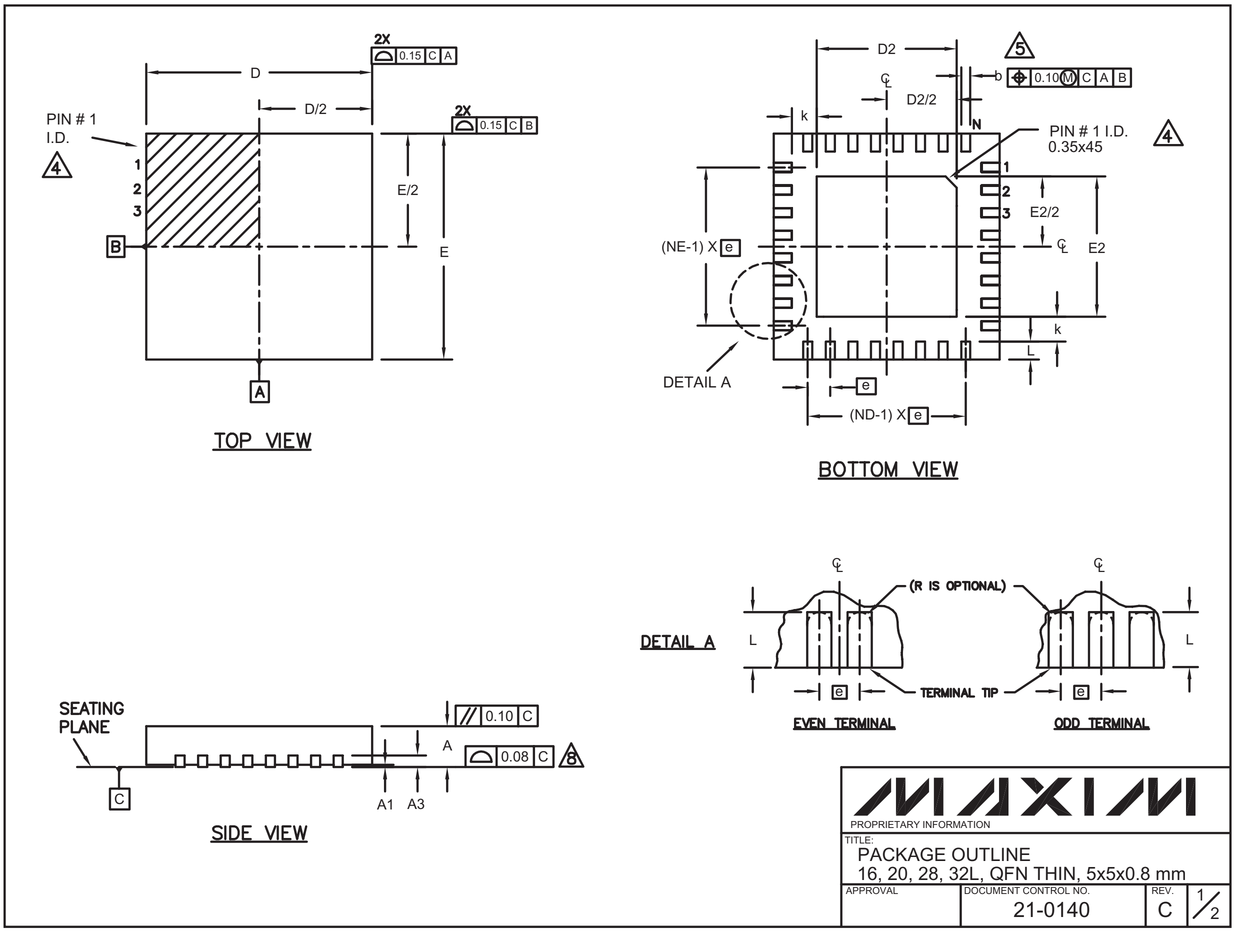
825MHz to 915MHz, SiGe High-Linearity Active Mixer

Typical Application Circuit



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



825MHz to 915MHz, SiGe High-Linearity Active Mixer

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm

APPROVAL | DOCUMENT CONTROL NO. 21-0140 | REV. C | 2/2

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